AMENDMENTS TO THE CLAIMS

1-24. (Canceled)

25. (New) A noise-reducing transistor arrangement, comprising:

a first and a second field effect transistor, each of which has a source terminal, a drain terminal, and a control terminal for application of a first signal or a second signal;

wherein the source terminal of the first field effect transistor and the source terminal of the second field effect transistor are coupled to one another, and wherein the drain terminal of the first field effect transistor and the drain terminal of the second field effect transistor are coupled to one another, and

a clock generator unit, which is coupled to the field effect transistors such that the clock generator unit provides the first signal and the second signal alternately to the field effect transistors with an alternating frequency which is at least as great as the cut-off frequency of the noise characteristic of the field effect transistors, or with a reciprocal alternating frequency which is less than a mean lifetime of an occupation state of a defect in the boundary region between channel region and gate insulating layer of the field effect transistors,

applies the first signal to the control terminal of the first field effect transistor and, simultaneously, the second signal to the control terminal of the second field effect transistor, and

applies the second signal to the control terminal of the first field effect transistor and, simultaneously, the first signal to the control terminal of the second field effect transistor.

26. (New) The transistor arrangement as claimed in claim 25, wherein the control terminal is a gate terminal or a substrate terminal.

27. (New) The transistor arrangement as claimed in claim 25, wherein:

for a case where the control terminal of the first and of the second field effect transistor is a gate terminal, the first field effect transistor and the second field effect transistor have a substrate terminal as additional control terminal,

for a case where the control terminal of the first field effect transistor and of the second field effect transistor is a substrate terminal, the first field effect transistor and the second field effect transistor have a gate terminal as an additional control terminal, and

the additional control terminals of the first field effect transistor and of the second field effect transistor are coupled to one another.

28. (New) The transistor arrangement as claimed in claim 25, wherein one of the first and second signals is a useful signal and the respective other signal is a reference potential, or in which the first signal and the second signal are in each case a reference potential.

29. (New) The transistor arrangement as claimed in claim 25, wherein the first field effect transistor and the second field effect transistor are structurally identical.

30. (New) The transistor arrangement as claimed in claim 25, wherein the first signal and the second signal are applied alternately to the control terminal of the first field effect transistor and second field effect transistor, respectively, with an alternating frequency which is greater than the frequencies of a useful frequency band of an assigned circuit.

31. (New) The transistor arrangement as claimed in claim 26, wherein at least one of the substrate terminals is set up as a well terminal of one of the two field effect transistors, which is formed in a well.

32. (New) The transistor arrangement as claimed in claim 25, wherein both field effect transistors are of the same conduction type.

33. (New) The transistor arrangement as claimed in claim 32, wherein both field effect transistors are n-MOS transistors.

34. (New) The transistor arrangement as claimed in claim 32, wherein both field effect transistors are p-MOS transistors.

35. (New) The transistor arrangement as claimed in claim 25, which is set up such that a respective one of the two field effect transistors can be operated at an inversion operating point and the respective other of the two field effect transistors can be operated at an accumulation or depletion operating point.

36. (New) The transistor arrangement as claimed in claim 25, wherein:

the control terminal of the first field effect transistor is coupled to a first switching element, which can be switched by means of a first clock signal with an alternating frequency,

the control terminal of the second field effect transistor is coupled to a second switching element, which can be switched by means of a second clock signal, which is complementary to the first clock signal, with the alternating frequency, and

it is possible, by means of the respective switching elements, for the first or the second signal to be alternately applied to the respective control terminal of the respective field effect transistor with the alternating frequency.

37. (New) The transistor arrangement as claimed in claim 36, wherein the first switching element and the second switching element are a first switching transistor arrangement and a second switching transistor arrangement, respectively, to the respective gate terminal of which the respective clock signal can be applied, and a respective source/drain terminal of a respective switching transistor being coupled to the control terminal of the respective field effect transistor.

38. (New) The transistor arrangement as claimed in claim 25, which is formed on and/or in a silicon on insulator substrate.

39. (New) The transistor arrangement as claimed in claim 25, which is realized using analog circuit technology.

40. (New) The transistor arrangement as claimed in claim 38, further comprising at least one additional field effect transistor,

wherein each of the at least one additional field effect transistor has a source terminal and a drain terminal and also has a control terminal, to which the first signal or the second signal can be applied,

wherein the source terminal of the first field effect transistor and the source terminal of the second field effect transistor are coupled to the source terminal of each of the at least one additional field effect transistors,

wherein the drain terminal of the first field effect transistor and the drain terminal of the second field effect transistor are coupled to the drain terminal of each of the at least one additional field effect transistors, and

wherein the transistor arrangement is set up such that, in a first operating state, the first signal is applied to the control terminal of the first field effect transistor or of the second field effect transistor or of precisely one of the at least one additional field effect transistor and, simultaneously, the second signal is applied to the control terminals of all of the other field effect transistors, in subsequent operating states, the first signal being applied progressively to the control terminal of in each case one of the remaining field effect transistors and, simultaneously, the second signal being applied to the control terminals of all of the other field effect transistors.

41. (New) The transistor arrangement as claimed in claim 25, wherein the clock generator unit is set up such that it provides the signals to the field effect transistors alternately by means of clock signals that are shifted relative to one another.

42. (New) The transistor arrangement as claimed in claim 40, wherein the clock generator unit is set up such that it prescribes the clock signals for reducing the heating of the field effect transistors formed on and/or in the silicon on insulator substrate and/or for reducing the floating body effect of the field effect transistors formed on and/or in the silicon on insulator substrate.

43. (New) An integrated circuit comprising at least one transistor arrangement as claimed in claim 25.

44. (New) The integrated circuit as claimed in claim 43, set up as one of a differential stage circuit, a current source circuit, a current mirror circuit, and an operational amplifier circuit.

45. (New) The integrated circuit as claimed in claim 43, set up as a current source circuit, wherein the drain terminal of the first field effect transistor and the drain terminal of the second field effect transistor are at ground potential.

46. (New) The integrated circuit as claimed in claim 43, set up as a current source circuit, and further comprising a voltage source, wherein the drain terminal of the first field effect transistor and the drain terminal of the second field effect transistor are brought to a potential that is different from ground potential by means of the voltage source.

47. (New) The integrated circuit as claimed in claim 43, set up as a cascaded current source circuit.

48. (New) The transistor arrangement as claimed in claim 25, wherein the gate terminal of the first field effect transistor and the gate terminal of the second field effect transistor are coupled to one another.

49. (New) The transistor arrangement as claimed in claim 48, wherein the well terminal of the first field effect transistor and the well terminal of the second field effect transistor are provided separately from one another.

50. (New) A method of reducing the noise of field effect transistors, comprising:

connecting a first field effect transistor and a second field effect transistor to one another, each of the field effect transistors having a source terminal and a drain terminal and also a control

terminal for application of a first or a second signal, wherein the source terminal of the first field effect transistor and the source terminal of the second field effect transistor are coupled to one another, and wherein the drain terminal of the first field effect transistor and the drain terminal of the second field effect transistor are coupled to one another; and

applying the first signal and the second signal alternately to the field effect transistors with an alternating frequency which is at least as great as the cut-off frequency of the noise characteristic of the field effect transistors, or with a reciprocal alternating frequency which is less than a mean lifetime of an occupation state of a defect in the boundary region between channel region and gate insulating layer of the field effect transistors, wherein the applying step comprises:

applying the first signal to the control terminal of the first field effect transistor and, simultaneously applying the second signal to the control terminal of the second field effect transistor; and

applying the second signal to the control terminal of the first field effect transistor and, simultaneously applying the first signal to the control terminal of the second field effect transistor.

51. (New) The method as claimed in claim 50, wherein a gate terminal or a substrate terminal is used as the control terminal.

52. (New) The method as claimed in claim 51, wherein, by means of the alternating application of the first and second signals, the quasi-Fermi energy in a boundary region between channel region and gate insulating layer of the field effect transistors is periodically altered by a value which is greater than the product of the Boltzmann constant and the absolute temperature.

53. (New) The method as claimed in claim 51, wherein, by means of the alternating application of the first and second signals, the quasi-Fermi energy in a boundary region between channel region and gate insulating layer of the field effect transistors is periodically altered by between approximately 100 meV and approximately 1 eV.

54. (New) The method as claimed in claim 50, wherein the arrangement of the field effect transistors is formed on and/or in a silicon on insulator substrate.

55. (New) The method as claimed in claim 50, wherein the first signal and the second signal are applied alternately to the control terminals of the first field effect transistor and of the second field effect transistor in such a way that the heating of the field effect transistors formed on and/or in the silicon on insulator substrate is reduced and/or the floating body effect of the field effect transistors formed on and/or in the silicon on insulator substrate is reduced.